FORM PTO-1390 (REV. 11-2000) — US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
P/61715-PCT	10/019140

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/GB00/02200	June 7, 2000	June 25, 1999

TITLE OF INVENTION **REFLECTING MODULATOR CIRCUIT COMPRISING A NEGATIVE IMPEDANCE AMPLIFIER**

APPLICANT(S) FOR DO/EO/US **Ian James FORSTER, Adrian Nigel FARR**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under ~~35 U.S.C. 371.~~
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This is an express request to begin national examination procedures (35 U.S.C. 371 (f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [X] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information: **Receipt Acknowledgment Postcard**

U.S. APPLICATION NO (if known, see 37 CFR 1.5) 10/069140	INTERNATIONAL APPLICATION NO PCT/GB00/02200	ATTORNEY'S DOCKET NUMBER P/61715-PCT

21. [X] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,040.00		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $740.00		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $710.00		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	$0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	10 - 20 =	0	x **$18.00**	$0.00	
Independent claims	3 - 3 =	0	x **$84.00**	$0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$890.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$0.00	
SUBTOTAL =				$890.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$0.00	
TOTAL NATIONAL FEE =				$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21 (h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$0.00	
TOTAL FEES ENCLOSED =				$890.00	
				Amount to be refunded:	$
				charged:	$

a. [X] A check in the amount of **$890.00** to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-1145. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

KIRSCHSTEIN, OTTINGER, ISRAEL & SCHIFFMILLER, P.C.
489 Fifth Avenue
New York, New York 10017
(212) 697-3750

SIGNATURE:

Alan Israel
NAME
27,564
REGISTRATION NUMBER

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail No. EL 337 911 808 US in an envelope addressed to: Box: PCT, Commissioner of Patents and Trademarks, Washington, D.C., 20231, on:
December 20, 2001
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PATENTS
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December 20, 2001
(date)
Alan Israel
Reg. No. 27,564

International Application No.: PCT/GB00/02200

International Filing Date : June 7, 2000

In re: Application of : Ian James FORSTER

Deposited : December 20, 2001

For : REFLECTING MODULATOR CIRCUIT COMPRISING A NEGATIVE IMPEDANCE AMPLIFIER

New York, New York
December 20, 2001

PRELIMINARY AMENDMENT

BOX: PCT
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to calculation of the filing fee and before examination, kindly amend the above captioned application as follows:

IN THE CLAIMS:

Please cancel claims 1-10, without prejudice.

Please add the new set of claims set forth on the enclosed pages.

IN THE ABSTRACT:

Delete the "Abstract"on the PCT cover sheet and replace it with the "Abstract of the Disclosure" set forth on a separate sheet attached hereto.

REMARKS

An abstract has been provided on a separate sheet; and the claims have been amended to conform to U.S. practice.

Wherefore, an early action on the merits is earnestly solicited.

Respectfully submitted,

KIRSCHSTEIN, OTTINGER, ISRAEL & SCHIFFMILLER, P.C.
Attorneys for Applicant(s)
489 Fifth Avenue
New York, New York 10017-6105
Tel: (212) 697-3750
Fax: (212) 949-1690

Alan Israel
Registration No. 27,564

ABSTRACT OF THE DISCLOSURE

A modulator circuit comprises a negative impedance amplifier which is operable such that a signal applied to the amplifier is reflected and amplified. Switching circuitry is provided for switching the impedance of the amplifier between two reflecting states such that the reflected and amplified signal is phase modulated. The impedances of the negative impedance amplifier are selected such that the phase of the reflected and amplified signal switches by substantially 180°. Preferably, the impedances of the negative impedance amplifier in the two reflecting states are selected such that the reflection gain of the amplifier in the two reflecting states is substantially the same such that the reflected and amplified signal is a binary phase shift keyed.

PROPOSED NEW CLAIMS

11. A modulator circuit, comprising: a negative impedance amplifier operable for reflecting and amplifying a signal applied to the amplifier; and switching means for switching the impedance amplifier between two reflecting states having impedances in the two reflecting states selected such that a phase of a reflected and amplified signal switches by substantially 180°.

12. The modulator circuit according to claim 11, in which the impedances in the two reflecting states are selected such that a reflection gain of the amplifier in the two reflecting states is substantially the same and such that the reflected and amplified signal is a binary phase shift keyed signal.

13. The modulator circuit according to claim 11, in which the impedances in the two reflecting states are selected such that a reflection gain of the amplifier in the two reflecting states is different, and wherein the impedances are selected such the reflected and amplified signal is a substantially single sideband signal.

14. The modulator circuit according to claim 11, in which the negative impedance amplifier comprises a transistor, and a biasing means for biasing the transistor such as to act as the negative impedance amplifier.

15. The modulator circuit according to claim 14, in which the switching means switches the biasing of the transistor to switch the transistor between the two reflecting states.

16. The modulator circuit according to claim 11, and further comprising an antenna for receiving and converting radiation to the signal applied to the amplifier, and for radiating the reflected and amplified signal.

17. The modulator circuit according to claim 14, in which the transistor comprises a bipolar transistor.

18. The modulator circuit according to claim 14, in which the transistor comprises a field effect transistor.

19. A de-modulator circuit for de-modulating a binary phase shift keyed signal, comprising: a modulator circuit including a negative impedance amplifier operable for reflecting and amplifying a signal applied to the amplifier; and switching means for switching the impedance amplifier between two reflecting states having impedances in the two reflecting states selected such that a phase of a reflected and amplified signal switches by substantially 180°.

20. A transponder tag, comprising: a modulator circuit including a negative impedance amplifier operable for reflecting and amplifying a signal applied to the amplifier; and switching means for switching the impedance amplifier between two reflecting states having impedances in the two reflecting states selected such that a phase of a reflected and amplified signal switches by substantially 180°.

REFLECTING MODULATOR CIRCUIT COMPRISING A NEGATIVE IMPEDANCE AMPLIFIER

This invention relates to a modulator circuit and more especially to such a circuit for generating binary phase shift key modulation.

Modulation, which can be broadly defined as a time varying modification of a signal to impart information thereto, is a crucial feature of the design of almost all radio based systems. An effective and well known form of modulation for digital signals, is binary phase shift keying (BPSK). In BPSK one of the two digital states of information is imparted onto a carrier signal by modulating its phase to have two discrete values which are generally separated by 180 degrees (π radians). Whilst such a modulation technique may be efficient it has not previously been ideally suited for applications where low cost and low power consumption are paramount such as in tagging systems, since the known circuitry for generating BPSK is complex and consumes too much electrical power for operation from a finite battery supply.

The present invention has arisen in an endeavour to provide a modulator circuit which at least in part overcomes the limitations of the known modulators and which is suitable for use in a tagging systems or other applications where low power consumption and circuit simplicity are of importance.

According to the present invention a modulator circuit comprises: a negative impedance amplifier operable such that a signal applied to the amplifier is reflected and amplified and switching means for switching the impedance of the amplifier between two

reflecting states, characterised in that the impedances in the two reflecting states are selected such that the phase of the reflected and amplified signal switches by substantially 180 degrees.

Preferably the impedances in the two reflecting states are selected such that the reflection gain of the amplifier in the two reflecting states is substantially the same such that the reflected and amplified signal is a binary phase shift keyed.

Alternatively the impedances in the two reflecting states are selected such that the reflection gain of the amplifier in the two reflecting states is different and wherein said impedances are selected such the reflected and amplified signal is a substantially single sideband signal.

In a particularly preferred embodiment the negative impedance amplifier comprises a transistor, such as for example a bipolar or field effect transistor, and biasing means for biasing the transistor such as to act as a negative impedance amplifier. Such a modulator circuit is found to be particularly advantageous since it in essence can comprise only a single component. Furthermore, a negative impedance amplifier is capable of providing high gain at very low current, so its power consumption can accordingly be very low of the order of a few micro-amps. Conveniently when using a transistor the switching means switches the biasing of the transistor to switch the transistor between the two reflecting states.

Advantageously the modulator circuit further comprises an antenna for receiving

radiation and converting it to the signal applied to the amplifier and for radiating the reflected and amplified signal.

According to a second aspect of the invention there is provided a demodulator circuit for demodulating a Binary phase shift keyed signal which incorporates the modulator circuit described above.

According to a third aspect of the invention there is provided a transponder tag which incorporates the modulator circuit described above.

A modulator circuit in accordance with the invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a schematic representation of a transponder circuit which incorporates a modulator circuit in accordance with the invention;

Figure 2 is a schematic representation of a de-spreader circuit for use in a spread spectrum communication system which incorporates the modulator circuit of Figure 1; and

Figure 3 is a schematic representation of a spread spectrum communication system incorporating the modulator circuit of Figure 1.

Referring to Figure 1 there is shown a microwave frequency (2.45 GHz) pseudo passive

transponder tag 1 for use in a tagging system which incorporates a modulator circuit 2 in accordance with the invention. The tag 1 comprises an antenna 4 which is connected to the modulator circuit 2. The modulator circuit 2 comprises: a gallium arsenide (GaAs) field effect transistor (FET) 6, impedance matching/feedback networks 8,10,12 connected to a respective transistor terminal, a switchable current source 14 and a control circuit 16. The antenna 4, which for operation at microwave frequencies conveniently comprises a patch antenna, is connected to the gate electrode 6_g of the FET 6 via the matching network 8 which conveniently comprises a transmission line element. The drain electrode 6_d of the FET 6 is connected to a positive supply V_{supply} by the matching network 10. The source electrode 6_s connected to ground via the matching network 12 and the switchable current source 14. The current source 14 is controlled by the control circuit 16 via a control line 18.

In a known manner the FET 6 is biased by a biasing network which comprises the matching/feedback networks 8, 10, 12 such that it operates in a linear relatively high gain region of its current/voltage characteristic. Conveniently each of the networks 8,10,12 comprises a transmission line element. The FET 6 thus amplifies and reflects any signal appearing at its gate electrode 6_g and therefore acts as a negative impedance amplifier. This being said, it will be appreciated that in most applications the impedance of the amplifier is primarily resistive.

The magnitude of the negative impedance of the modular circuit 2 is dependent on the drain/source current I_{ds} passing through the transistor 6 and this current is determined by the switchable current source 14. The current source 14 is switchable between two

selected currents I_{ds1} and I_{ds2} in dependence upon control circuit 16. For both currents I_{ds1} and I_{ds2} the FET 6 operates as a negative impedance amplifier though for each current the magnitude of its negative impedance is different.

In operation of the circuit 1 the antenna 4 receives and converts microwave radiation 19 into an electrical signal which is applied via the matching network 8 to the gate 6_g of the FET 6. As described above the FET 6 acts as a negative impedance amplifier and the electrical signal is reflected and amplified by the FET 6 and re-radiated as microwave radiation 20 from the antenna 4. In the case of tagging systems the microwave radiation 19 is an interrogating radiation signal which can be a continuous wave or modulated wave signal. To impart information to the radiation 20 the control circuit 16 switches between the two currents I_{ds1} and I_{ds2} such that the phase of the radiation 20 switches by 180 degrees. An important feature of the invention is the selection of the magnitude of the negative impedance of the circuit 2 for the two currents I_{ds1} and I_{ds2}. These are selected such that (i) the circuit has the same reflection gain for each current and (ii) the phase between the reflected and amplified signal for the two currents is switched by 180 degrees. The reflection gain (in decibels dB) of the circuit 1 as seen looking toward the gate terminal 6_g is given by:

$$\text{gain} = 20 \log \left| \frac{Zn - Zo}{Zn + Zo} \right|$$

where Zo is the antenna impedance (or in the case where no antenna is present, it is the system impedance) and Zn is the input impedance presented by the FET 6 (that is the negative impedance looking towards the gate 6_g). For the embodiment shown in Figure

l the system/antenna impedance is nominally 50 ohms and the value of the negative impedance is switchable between -45 and -55.555 ohms for I_{ds1} and I_{ds2} respectively to give a reflection gain in each case of 25dB. It is to be noted that for these impedance values whilst the reflection gain is constant, the phase of the reflected and amplified signals will be altered by 180 degrees. This change of phase is indicated by the change of the sign of the term (Zn-Zo) ÷ (Zn + Zo). Thus for the example of Figure 1 I_{ds1} is selected such that the FET 6 operates as a negative impedance of -45 ohms and I_{ds2} is selected such that the FET 6 operates as negative impedance of -55.555 ohms. It will be appreciated therefore that the circuit 2 acts as a binary phase shift key reflective modulator. A particular advantage of the modulator circuit 2 is that it provides a simple method of generating BPSK and offers the additional benefit that it also amplifies the signal which it is modulating. Due to the circuit's simplicity it is ideally suited to tagging applications where it further has the advantage that it is capable of operating at very low currents (of the order of a few micro-amps) for an operating frequency of 2.4GHz.

With different values for the respective impedances, both the magnitude and phase of the reflected signal can be varied between the two states, such that a combination of amplitude modulation (AM) and phase modulation (PM) can be applied. With an appropriate combination of the two forms of modulation the radiated signal 20 can be arranged to be a substantially single sideband signal.

Referring to Figure 2 there is shown a schematic of a de-spreader circuit 21 for use in a spread spectrum communication system such as for example of the type used in a

global positioning system. As is known in such spread spectrum systems a carrier signal is modulated with a digital code, most often a pseudo random binary sequence (PRBS), to spread its energy spectra. Commonly the modulation used is BPSK. The circuit 21 is intended for de-spreading such spread spectrum radiation to recover the original carrier signal and any modulation applied thereto. This is achieved by using the modulator 2 of Figure 1 to apply a replica of the sequence used to generate the spread spectrum. It will be appreciated that the sequence applied by the circuit 21 is additionally in time synchronisation with the generating sequence.

The circuit 21 comprises; an antenna 22 for receiving broad band spread spectrum radiation 23, a broad pass-band filter 24, a narrow stop-band filter 25, a narrow pass-band filter 26 and a modulator circuit 2. The broad pass-band filter 24, narrow stop-band filter 25 and narrow pass-band filter 26 are connected in series and the output 28 of the narrow pass-band filter 26 provides the output 28 of the circuit 21. The antenna 22 is connected to the input 30 of the broad band filter 24. The modulator circuit 2, which is identical to the circuit shown in Figure 1, is connected to the interconnection 32 of the filters 25 and 26.

The reflective modulator circuit 2 has a gain of 20dB in both reflecting states. The reflecting state of the modulator 2 is controlled by a digital signal 34, which as described above is a replica of the original sequence signal used to generate the broad band signal 23. Most typically the signal 34 is a PRBS signal.

In operation the broad band spread radiation 23 is received and converted to an

electrical signal by the antenna 22 and passes through the broad pass-band filter 24 and narrow stop-band filter 25. The pass-band of the filter 24 defines the bandwidth of operation of the circuit 21. The centre frequency of the stop-band filter 25 is selected to correspond with the carrier frequency of the radiation 23 to block any components at the carrier frequency. The filtered signal appearing at the output 32a of the filter 25 is applied to both the input 32b of the narrow pass-band filter 26 and to the input 32c of the modulator 2. Due to the pass-band pass characteristic of the narrow band-pass filter 26 the filtered signal is blocked by the filter 26. The filtered signal however appearing at the input 32c of the modulator circuit 2 is de-modulated to produce an amplified version of the original carrier signal which is reflected back to the interconnection 32. The amplified carrier signal, which is within the band pass characteristic of the narrow pass-band filter 26, passes through substantially unattenuated to the output 28. The demodulated signal is prevented from returning to the antenna 22 by the stop-band filter 25. The circuit 20 thus operates as a de-spreader circuit and is capable of operating at substantially lower currents than those which currently use digital techniques.

A further example of an application of the reflector modulator in accordance with the invention is now described with reference to Figure 3 which is a schematic of a spread spectrum communication system 40 for use in covert communications between a transmitter 42 and a hand held radio receiver 44. As is known spreading the spectra of the transmitted signal, and hence spreading the energy over a large frequency range, makes it more difficult for the signal to be detected by unauthorised persons and hence for such persons to determine the position of the transmitting source.

Referring to Figure 3 the communication system 40 comprises: a spread spectrum transmitter 42 of a known type which generates a BPSK modulated broad band spread spectrum radiation 46, a reflective de-spreading circuit 48 and a hand held radio receiver 44. The de-spreader circuit 48 is identical to the transponder circuit 1 of Figure 1 in which the control circuit 16 switches the transistor 6 using an identical code to that used by the transmitter 42 to generate the spread signal 46. The de-spreader circuit 48 thus receives the broad band radiation 46 and in response radiates an amplified and de-spread narrow band radiation 50 which represents the recovered carrier of the signal 46 and any modulation applied thereto. The narrow band radiation 50 is detected by the hand held radio receiver 44. The de-spreading circuit 48 is preferably mounted at a high point such as on the side of a building 52 or other structure such as a post or a tree. Since the radiation 46 generated by the transmitter 42 is broad band this makes it difficult for a direction finding receiver to locate the position of the transmitter 42. Although such a direction finding receiver may be able to locate the narrow band radiated emissions 50 from the de-spreading circuit 48 and hence determine its position, it will still be unable to determine the position of the transmitter 42. In a preferred communication system a number of de-spreading circuits 48 (a second such circuit 48a is shown in Figure 3), each having a different modulation code, are located at different physical locations. The transmitter 42 is operable to switch between the different modulating codes during communication with the hand held radio 44 such that different de-spreading circuits 48 become activated. As a result the position from which the narrow band radiation 50, 50a originates will jump from de-spreading circuit 48 to de-spreading circuit 48a, thereby hampering any attempt to locate the position of the de-spreading circuit.

It will be appreciated that modifications can be made to the circuits described which are still within the scope of the invention. For example whilst in the examples described the modulator circuit uses a field effect transistor, which is much preferred for operation of microwave frequencies, the negative impedance amplifier can be implemented in different ways, depending upon the required frequency of operation, such as for example using a bi-polar transistor or other active devices. Furthermore the modulator circuit of the invention is not restricted to the applications described and is suited for use in any application which requires BPSK modulation. The present invention resides in the realisation that binary phase shift key modulation can be achieved by using a reflection amplifier and switching the circuit between two reflecting states which preferably have the same reflection gain (though this is not essential when single sideband operation is required), but which change the phase of the reflected signal by substantially 180 degrees.

CLAIMS

1. A modulator circuit (2)comprising: a negative impedance amplifier (6) operable such that a signal applied to the amplifier is reflected and amplified and switching means (14, 16) for switching the impedance of the amplifier(6) between two reflecting states, characterised in that the impedances in the two reflecting states are selected such that the phase of the reflected and amplified signal switches by substantially 180 degrees.

2. A modulator circuit according to Claim 1 in which the impedances in the two reflecting states are selected such that the reflection gain of the amplifier (6) in the two reflecting states is substantially the same such that the reflected and amplified signal is a binary phase shift keyed.

3. A modulator circuit according to Claim 1 in which the impedances in the two reflecting states are selected such that the reflection gain of the amplifier (6) in the two reflecting states is different and wherein said impedances are selected such the reflected and amplified signal is a substantially single sideband signal.

4. A modulator circuit according to Claim 1 or Claim 2 in which the negative impedance amplifier comprises a transistor (6) and biasing means (10, 12, 14) for biasing the transistor such as to act as negative impedance amplifier.

5. A modulator circuit according to Claim 4 in which the switching means (14, 16) switches the biasing of the transistor (6) to switch the transistor between the two reflecting states.

6. A modulator circuit according to any preceding claim and further comprising an antenna (4) for receiving radiation (19) and converting it to the signal applied to the amplifier (6) and for radiating (20) the reflected and amplified signal.

7. A modulator circuit according to any one of Claims 4, 5 or 6 in which the transistor (6) comprises a bipolar transistor.

8. A modulator circuit according to any one of Claims 4, 5 or 6 in which the transistor (6) comprises a field effect transistor.

9. A de-modulator circuit (21) for de-modulating a Binary Phase Shift Keyed signal incorporating a modulator circuit (2) according to any preceding claim.

10. A transponder tag incorporating a modulator circuit according to any preceding claim.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(71) Applicant *(for all designated States except US)*: MARCONI CASWELL LIMITED [GB/GB]; One Bruton Street, London W1X 8AQ (GB).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: FORSTER, Ian, James [GB/GB]; 31 Great Cob, Springfield, Chelmsford, Essex CM1 6LA (GB). FARR, Adrian, Nigel [GB/GB]; The Mill House, Bran End, Stebbing, Dunmow, Essex CM6 3RS (GB).

(74) Agent: HOSTE, Colin, Francis; Marconi Intellectual Property, Waterhouse Lane, Chelmsford, Essex CM1 2QX (GB).

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Published:
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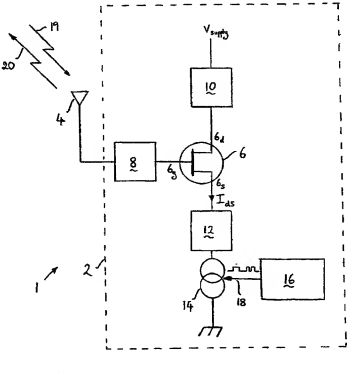
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: REFLECTING MODULATOR CIRCUIT COMPRISING A NEGATIVE IMPEDANCE AMPLIFIER



(57) Abstract: A modulator circuit comprises a negative impedance amplifier (6) which is operable such that a signal applied to the amplifier (6) is reflected and amplified. Switching means (14, 16) are provided for switching the impedance of the amplifier (6) between two reflecting states such that the reflected and amplified signal is phase modulated. The impedances of the negative impedance amplifier are selected such that the phase of the reflected and amplified signal switches by substantially 180 degrees. Preferably the impedances of the negative impedance amplifier in the two reflecting states are selected such that the reflection gain of the amplifier in the two reflecting states is substantially the same such that the reflected and amplified signal is a binary phase shift keyed.

WO 01/01649 A1

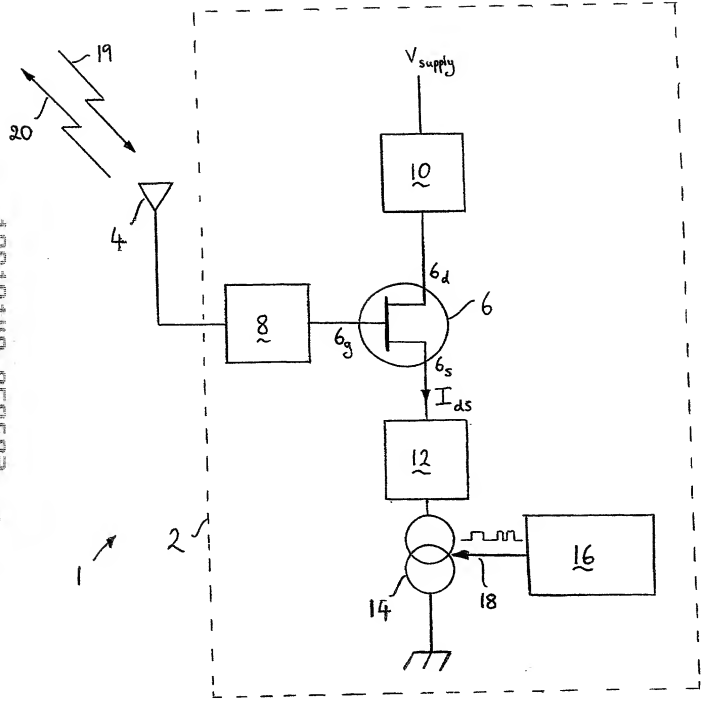


Figure 1.

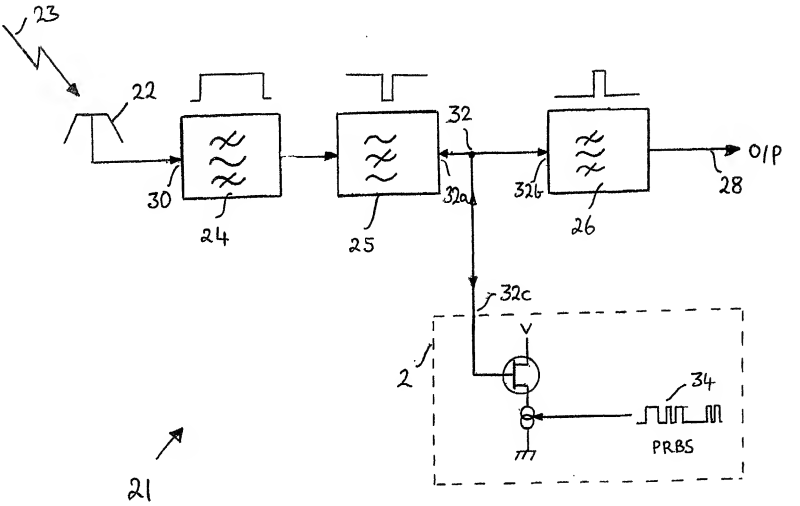


Figure 2.

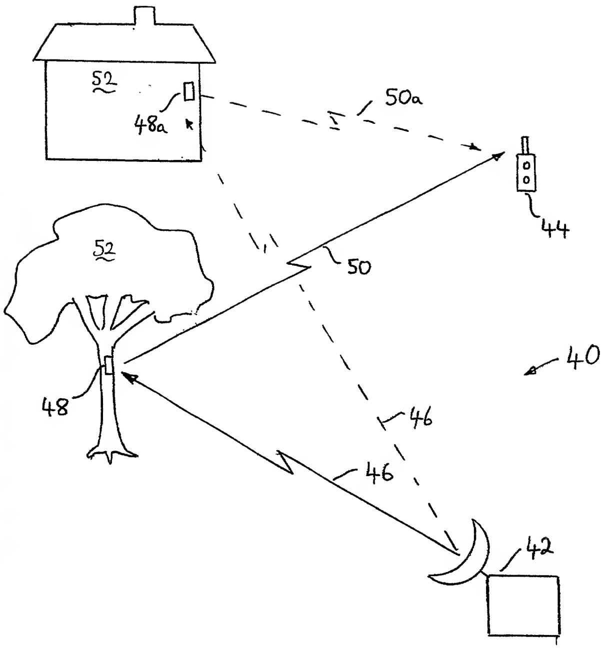


Figure 3

PTO/SB/01 (6-95)
Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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0010/PTO Rev. 6/95 — U.S. Department of Commerce, Patent and Trademark Office

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing

Attorney Docket Number	P/617/5
First Named Inventor	FORSTER, IAN JAMES
COMPLETE IF KNOWN	
Application Number	10/019,140
Filing Date	DECEMBER 20, 2001
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled :

REFLECTING MODULATOR CIRCUIT COMPRISING A NEGATIVE IMPEDANCE AMPLIFIER

(Title of the Invention)

the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) DECEMBER 20, 2001 as United States Application Number or PCT International

Application Number 10/019,140 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	Certified Copy Attached? NO
9914941.1	United Kingdom	June 25, 1999	☐	☐	☒
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
PCT/GB00/02300	INTERNATIONAL	June 7, 2000	☐	☐	☒

☐ Additional foreign application numbers are listed on a supplemental priority sheet attached hereto:

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority sheet attached hereto.

Burden Hour Statement: This form is estimated to take .4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

10019140 - 050502

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DECLARATION

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT International application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority sheet attached hereto.

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

☐ Firm Name OR ☒ List attorney(s) and/or agent(s) name and registration number below: Customer Number or label

Name	Registration Number	Name	Registration Number
David B. Kirschstein, Esq.	17,244		
Alan Israel, Esq.	27,564		
Martin W. Schiffmiller, Esq.	30,421		

☐ Additional attorney(s) and/or agent(s) named on a supplemental sheet attached hereto.

Please direct all correspondence to: ☐ Customer Number or label | OR ☒ Fill in correspondence address below

Name KIRSCHSTEIN, OTTINGER, ISRAEL & SCHIFFMILLER, P.C.
Address 489 Fifth Avenue
Address
City New York **State** New York **ZIP** 10017-6105
Country United States **Telephone** (212) 697-3750 **Fax** (212) 949-1690

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name	Middle Initial	Family Name	Suffix e.g. Jr.
Adrian	N	FARR	

Inventor's Signature [signature] GBX **Date** 23/1/2002

Residence: City Stebbing, Dunmow **State** **Country** United Kingdom **Citizenship** British

Post Office Address The Mill House, Bran End, Stebbing, Dunmow, Essex, CM6 3RS, (GB) UK

Post Office Address

City Stebbing, Dunmow **State** **ZIP** CM6 3RS **Country** United Kingdom **Applicant Authority**

☒ Additional inventors are being named on supplemental sheet(s) attached hereto

10019140-050602

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name	Ian	Middle Initial	J	Family Name	FORSTER	Suffix e.g. Jr.	
Inventor's Signature	X [signature] GB X			Date	X 21st January 2002		
Residence: City	Springfield, Chelmsford	State		Country	United Kingdom	Citizenship	British
Post Office Address	31 Great Cob, Springfield, Chelmsford, Essex, CM1 6LA, (GB) UK						
Post Office Address							
City	Springfield, Chelmsford	State		Zip	CM1 6LA	Country	United Kingdom
Applicant Authority							

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name		Middle Initial		Family Name		Suffix e.g. Jr.	
Inventor's Signature				Date			
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		Zip		Country	
Applicant Authority							

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name		Middle Initial		Family Name		Suffix e.g. Jr.	
Inventor's Signature				Date			
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		Zip		Country	
Applicant Authority							

Name of Additional Joint Inventor, if any: ☐ A petition has been filed for this unsigned inventor

Given Name		Middle Initial		Family Name		Suffix e.g. Jr.	
Inventor's Signature				Date			
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		Zip		Country	
Applicant Authority							

☐ Additional inventors are being named on supplemental sheet(s) attached hereto